THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIGERU ATSUMI, HIRONORI BANBA
and MASAO KURIYAMA

Appeal No. 1997-4092
Application No. 08/181,404

HEARD: February 23, 2000

Before, HAIRSTON, FLEMING and DIXON, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 26 and 30 through 51.

The disclosed invention relates to a nonvolatile semiconductor memory system that comprises a nonvolatile memory cell array divided into refresh blocks, and a flag cell

array including a plurality of flag cells. Each of the flag cells corresponds to one of the refresh blocks, and stores data representing refresh status of the corresponding refresh block.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A nonvolatile semiconductor memory system comprising:

a nonvolatile memory cell array including a plurality of nonvolatile memory cells arranged in matrix, said nonvolatile memory cell array being divided into refresh blocks;

a flag cell array including a plurality of nonvolatile flag cells each of which corresponds to one of said refresh blocks and stores data representing refresh status of the corresponding refresh block.

The reference relied on by the examiner is:

Hollerbauer 5,283,885 Feb. 1, 1994
(effective filing date Apr. 12, 1989)

Claims 1 through 26 and 30 through 51 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hollerbauer.

Reference is made to the final rejection, the briefs and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 102(e) rejection of claims 1 through 26 and 30 through 51.

Appellants argue (Brief, pages 10 and 11) that "it is important to point out that Hollerbauer is directed to a dynamic RAM, while the claimed invention specifically recites a nonvolatile semiconductor memory system that includes a nonvolatile memory cell array and a flag cell array including a plurality of nonvolatile flag cells." Appellants recognize that claims 33 through 51 are not limited to a nonvolatile memory cell array and a plurality of nonvolatile flag cells and argue (Brief, page 19) that these claims include "flag cells each storing refresh status data corresponding to a respective one of the refresh blocks." "In complete contrast to the claimed invention, Hollerbauer teaches use of a plurality of registers that store start and stop addresses corresponding to portions of the dynamic RAM where data is stored" (Brief, page 19).

We agree with appellants' arguments. The examiner's statement (Answer, page 3) that "[e]ven though Hollerbauer's memory device is preferably constructed as a dynamic RAM

because a dynamic RAM requiring refresh is less expensive than EEPROM (a nonvolatile memory) it's application to a nonvolatile memory such as EEPROM is clearly recognized from the teachings of Hollerbauer (see columns 1-2)" is an admission that Hollerbauer discloses a volatile memory cell array (i.e., a dynamic RAM device) as opposed to a nonvolatile memory cell array. For this reason, we will not sustain the 35 U.S.C. § 102(e) rejection[1] of claims 1 through 26 and 30 through 32. After all, to anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. See Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1043, 1047, 34 USPQ2d 1565, 1567 (Fed. Cir. 1995).

All of the claims on appeal state that each of the flag cells stores refresh status data for a corresponding refresh block. According to the examiner (Answer, page 6), "Hollerbauer clearly shows the . . . steps of storing refresh status data in a nonvolatile flag cell array 32-34, selecting

[1] It appears that the examiner's reasons for rejecting the claims on appeal are more supportive of an obviousness rejection than an anticipation rejection.

a refresh block 29-31 according to the refresh status data in the nonvolatile flag cell array 32-34, and refreshing data stored in each memory cell of the selected refresh block 29-31." In the absence of evidence in the record, or a convincing line of reasoning by the examiner, that the start and stop addresses (column 2, lines 40 through 47; column 3, lines 48 through 62; column 4, lines 55 through 66; column 9, lines 3 through 24; column 10, lines 24 through 62; and column 11, lines 5 through 8) stored in the registers 11 (Figure 3 embodiment), in the reserved storage locations 32 through 34 (Figure 5 embodiment) or in the register storage locations 51 through 53 (Figure 6 embodiment) are the same as refresh status data, we will not sustain the 35 U.S.C. § 102(e) rejection of claims 1 through 26 and 30 through 51.

DECISION

The decision of the examiner rejecting claims 1 through 26 and 30 through 51 under 35 U.S.C. § 102(e) is reversed.

REVERSED

KENNETH W. HAIRSTON)

Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
MICHAEL R. FLEMING	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
	)	
JOSEPH L. DIXON	)	
Administrative Patent Judge	)	

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Appeal No. 1997-4092
Application No. 08/181,404

APJ HAIRSTON

APJ DIXON

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DECISION: REVERSED
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s):

Prepared: January 23, 2001

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK
DISK (FOIA) / REPORT